13. The integrated circuit memory of claim 11 wherein memory operations can be carried out simultaneously in the first and second memory banks.

14. The integrated circuit memory of claim 11 wherein each of the memory arrays in the first and second memory banks has substantially the same number of memory cells.

15. The integrated circuit memory of claim 11 wherein each of the plurality of memory arrays includes a plurality of memory cells arranged along rows and columns, the integrated circuit memory further comprising:

column selection circuit coupled to select columns of cells in response to column addresses; and

row selection circuit coupled to select rows of cells in response to row addresses,

wherein each of the plurality of mask options configures the row and column selection circuits to obtain a different partitioning of the plurality of memory arrays into the first and second memory banks.

16. The integrated circuit memory of claim 15 wherein the row and column selection circuits respectively receive a first row address and a first column address for accessing one or more memory cells in the first memory bank, and the row and column selection circuits respectively receive a second row address and a second column address for accessing one or more memory cells in the second memory bank.

17. The integrated circuit memory of claim 11 wherein the integrated circuit memory receives a first bank address and a second bank address, the first bank address including row and column addresses for accessing one or more memory cells in the first memory bank, and the second bank address including row and column addresses for accessing one or more memory cells in the second memory bank.

18. The integrated circuit memory of claim 11 wherein the one of a plurality of mask options corresponds to one of a plurality of metal masks used to form a metal layer in the integrated circuit.

19. An integrated circuit memory comprising:

a plurality of memory arrays each having memory cells arranged along rows and columns; and

reconfigurable row and column selection circuits coupled to access memory cells in the plurality of memory arrays in response to row and column addresses,

wherein one of a plurality of metal mask options is selected to configure the row and column selection circuits to obtain a desired partitioning of the plurality of memory arrays into first and second memory banks such that the first memory bank includes at least one but less than all of the plurality of memory arrays and the second memory bank includes a corresponding remainder of the plurality of memory arrays, and

wherein memory operations can be carried out simultaneously in the first and second memory banks.

20. The integrated circuit memory of claim 19 wherein each of the plurality of metal mask options corresponds to a different partitioning of the memory arrays into the first and second memory banks.

21. The integrated circuit memory of claim 19 wherein the integrated circuit memory receives a first bank address and a second bank address, the first bank address including row and column addresses for accessing one or more memory cells in the first memory bank, and the second bank address including row and column addresses for accessing one or more memory cells in the second memory bank.

22. An integrated circuit memory comprising:

a plurality of memory arrays each having memory cells arranged along rows and columns; and

reconfigurable row and column selection circuits coupled to access memory cells in the plurality of memory arrays in response to row and column addresses,

wherein the plurality of memory arrays are partitioned into first and second memory banks by configuring the row and column selection circuits into one of a plurality of mask-selectable configurations such that the first memory bank includes at least one but less than all of the plurality of memory arrays and the second memory bank includes a corresponding remainder of the plurality of memory arrays,

wherein each of the mask-selectable configurations corresponds to one of a plurality of metal masks used to form a metal layer in the integrated circuit.

23. A method of forming an integrated circuit memory, comprising:

forming a plurality of memory arrays; and

partitioning the plurality of memory arrays into first and second memory banks by selecting one of a plurality of mask options such that the first memory bank includes at least one but less than all of the plurality of memory arrays and the second memory bank includes a corresponding remainder of the plurality of memory arrays.

24. The method of claim 23 wherein each of the plurality of memory arrays includes a plurality of memory cells arranged along rows and columns, and the integrated circuit memory includes row and column selection circuits coupled to select memory cells in the plurality of memory arrays,

wherein the plurality of memory arrays are partitioned into first and second memory banks by configuring the row and column selection circuits into one of a plurality of mask-selectable configurations, each of the mask-selectable configurations corresponding to one of the plurality of mask options.

25. The method of claim 23 wherein each of the plurality of mask options corresponds to a different partitioning of the memory arrays into the first and second memory banks.

26. The method of claim 23 wherein memory operations can be carried out simultaneously in the first and second memory banks.

27. A method of manufacturing an integrated circuit memory having row and column selection circuits coupled to a plurality of memory arrays, the method comprising:

applying one of a plurality of metal masks to form a metal layer and to configure the row and column select circuits to obtain a desired partitioning of the plurality of memory arrays into first and second memory banks such that the first memory bank includes at least one but less than all of the plurality of memory arrays and the second memory bank includes a corresponding remainder of the plurality of memory arrays,

wherein each of the plurality of metal masks corresponds to a different configuration of the row and column selection circuits, and each of the different configurations of the row and column selection circuits correspond to a different partitioning of the plurality of memory arrays into the first and second memory banks.

REMARKS

Claims 1-10 are pending. Claims 1-10 are canceled, and new claims 11-27 are added. Support for the new claims can be found throughout the specification and the drawings.

35 USC 103(a) rejections

Claims 1-10 are rejected under 35 USC 103(a) as being unpatentable over Kuo et al. (USP 5,995,415) in view of Thummalapally et al. (USP 6,016,270). This

rejection is traversed in light of Applicant's canceling of claims 1-10 and adding of new clams 11-27

Claim 11 distinguishes over Kuo et al. and Thummalapally et al. taken singly or in combination, because neither reference teaches or suggests "a plurality of memory arrays partitioned into first and second memory banks in correspondence with one of a plurality of mask options such that the first memory bank includes at least one but less than all of the plurality of memory arrays and the second memory bank includes a corresponding remainder of the plurality of memory arrays".

Thus, claim 11 and its dependent claims 12-18 are allowable.

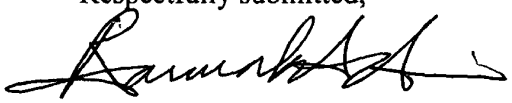
Each of the independent claims 19, 22, 23, and 27 includes a similar limitation to that of claim 11 recited above, and thus each of these claims and their respective dependent claims distinguish over Kuo et al. and Thummalapally et al. for at least the same reasons stated above in connection with claim 11.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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